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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,873	10/21/2005	Wlodek Kurjanowicz	PAT 2295W-2	1035

7590 11/13/2007

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
11/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,873	KURJANOWICZ, WLODEK	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *15-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,14 and 23-29* is/are rejected.

7)☒ Claim(s) *11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/23/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The preliminary amendment filed on October 21, 2005 has been entered.

Oath/Declaration

2. The oath/declaration filed on 10/21/2005 is acceptable.

Priority

3. Acknowledgement is made of applicant's claim for domestic priority under 35 U.S.C. 119(e), through provisional application 60/568,315 filed 05/06/2004.

Information Disclosure Statement

4. The Information Disclosure Statement filed on 01/23/2006 has been considered.

Election/Restrictions

5. Applicant's election without traverse of Group I (claims 1-14 and 23-29) in the reply filed on 10/19/2007 is acknowledged.

Drawings

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the field oxide region (claim 2), low voltage transistor (claim 3), high voltage transistor (claim 4) wordline decoding circuitry (claim 12), column select pass gate coupled (claim 14) to the bitlines (none of column select signals Y0-Y4 appear to be coupled to the bitlines), a length of the fusible edge is greater than a width of the active channel area (claim 26) and isolation edge (claim 29) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to under 37 CFR 1.83(a) because they fail to show "the edge consisting of two edge segments oriented at an angle with respect to each other" (page 15, lines 10 and 11) and "the edge consists of three edge segments oriented at 90 degree angles with respect to each other" (page 15, lines 20 and 21). It is requested that the edge segments be labeled with reference numerals. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is

figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 25 and 29 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The application as originally filed does not specifically support the claim limitation

"a length of the fusible edge is greater than a width of the active channel area." There is no discussion in the specification about a length of the fusible edge being greater than a width of the active channel area.

The application as originally filed does not specifically support the claim limitation "an isolation edge." There is no discussion in the specification about an isolation edge.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 3, 4, 8 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. The recitation of claim 3 calling for, "the thin gate oxide portion is identical to at least one low voltage transistor gate oxide formed on the semiconductor material," is not well understood. It is not clear whether the thin gate oxide is itself a gate oxide of a low voltage transistor or whether there exists a low voltage transistor next to a transistor which includes the thin gate oxide.

13. The recitation of claim 4 calling for, "the thick gate oxide portion is identical to at least one high voltage transistor gate oxide formed on the semiconductor material," is not well understood. It is not clear whether the high gate oxide is itself a gate oxide of a high voltage transistor or whether there exists a high voltage transistor next to a transistor which includes the thick gate oxide.

14. The recitation of claim 8 calling for, "the diffusion region has an LDD implant identical to the LDD implant of one of the low voltage transistor, the high voltage transistor, and a combination of both the low and the high voltage transistors" is not well understood. It is not clear whether the Ldd is itself an Ldd of a low/high/combination of both high and low voltage transistor or whether there exists a low/high/combination of both high and low next to a transistor which includes the Ldd implant.

15. The recitation of claim 14 calling for, "at least one of the column select pass gates having a gate oxide identical to the thick gate oxide portion," is not well understood. It is not clear whether the thick gate oxide is itself a gate oxide of a pass gate or whether there exists a pass gate next to a transistor which includes the thick gate oxide.

16. Claim 8 recites the limitation "the LDD implant of one ...." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

18. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Peng et al. ("Peng") US PG-Pub 2004/0156234.

Peng discloses in figs. 16 and 22-25 an anti-fuse transistor formed on a semiconductor material comprising: a polysilicon gate (par. 86) over a channel region in a substrate, the channel having a preset length; a diffusion region (see N+ implant adjacent the Normal Gox shown in fig. 16) proximate to a first end of the channel region (figs. 16, 22 and 23); an isolation region (see N+ implant adjacent the Thinner Gox shown in fig. 16) including floating diffusion region (**as recited in claim 2**) proximate to a second end of the channel region; a variable thickness gate oxide (Normal and Thinner Gox) between the polysilicon gate and the substrate, the variable thickness gate oxide having a thick gate oxide portion (Normal Gox) extending from the **first end** of the channel region to a predetermined distance of the preset length, a thin gate oxide portion (Thinner Gox) extending from the predetermined distance to the **second end** of the channel region (figs. 16, 22 and 23). Regarding the recitation calling for, "a breakdown resistant access edge proximate to the **first end** of the channel region for conducting current between the polysilicon gate and the diffusion region; and an oxide breakdown zone proximate to the **second end** of the channel region, the oxide breakdown zone fusible to form a conductive link between the polysilicon gate and the channel region," a prima facie case of anticipation has been established because the claimed and prior art products are identical or substantially identical in structure and/or composition. *In re Best,* 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product."). *See also In re Spada,* 911 F.2d 705, 708-09, 15 USPQ2d 1655, 1657-58 (Fed. Cir. 1990).

Re claim 3, Peng discloses (par. 91) the thin gate oxide portion is identical to at least one low voltage transistor gate oxide formed on the semiconductor material.

Re claim 4, Peng discloses (paragraphs 8 and 10) the thick gate oxide portion is identical to at least one high voltage transistor gate oxide formed on the semiconductor material.

The recitation of claim 5 calling for, "the thick gate oxide portion includes a combination of an intermediate gate oxide and the thin gate oxide portion" fails to further limit the anti-fuse structure.

Re the recitation of claim 6 calling for, "the floating diffusion region, the second end of the channel region and a gate edge of the polysilicon gate have a common edge defined by at least two line segments being at an angle to each other," a prima facie case of anticipation has been established because the claimed and prior art products are identical or substantially identical in structure and/or composition. *In re Best,* 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product."). *See also In re Spada,* 911 F.2d 705, 708-09, 15 USPQ2d 1655, 1657-58 (Fed. Cir. 1990).

Re the recitation of claim 7 calling for, "angle is one of 135 degrees and 90 degrees," a prima facie case of anticipation has been established because the claimed and prior art products are identical or substantially identical in structure and/or composition. *In re Best,* 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical

processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product."). *See also In re Spada,* 911 F.2d 705, 708-09, 15 USPQ2d 1655, 1657-58 (Fed. Cir. 1990).

Re claim 8, Peng discloses the diffusion region has an LDD implant (fig. 22) identical to the LDD implant of the low voltage transistor/the high voltage transistor (paragraphs 8, 10 and 91) which is one of the low voltage transistor, the high voltage transistor and a combination of both the low and the high voltage transistors.

Re claim 9, Peng discloses an edge of the diffusion region and a portion of the polysilicon gate is free of salicidation.

19. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Peng.

Peng discloses (abstract and figs. 16 and 22-25) anti-fuse memory array comprising: a plurality of anti-fuse transistors arranged in rows and columns, each anti-fuse transistor including a polysilicon gate (par. 86) over a channel region in a substrate, the channel having a preset length; a diffusion region (see N+ implant adjacent the Normal/Thinner Gox shown in fig. 16) proximate to a first end of the channel region; a variable thickness gate oxide (Normal/Thinner Gox) between the polysilicon gate and the substrate, the variable thickness gate oxide having a thick gate oxide portion (Normal Gox) extending from the first end of the channel region to a predetermined distance of the preset length, and a thin gate oxide portion (Thinner Gox) extending from the predetermined distance to a second end of the channel region an oxide breakdown zone proximate to the second end of the channel region; bitlines **WL** coupled to the diffusion regions of a column of anti-fuse transistors; and, wordlines BL coupled to the polysilicon gates of a row of anti-fuse transistors.

20. Claims 23, 24 and 26-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Peng.

Peng discloses in figs. 16 and 22-25 an anti-fuse transistor formed on a semiconductor material comprising: an active channel area; a polysilicon gate (par. 86) formed over the active channel area to define a fusible edge (adjacent Thinner Gox) to and an access edge (adjacent Normal Gox); a thick gate oxide (Normal Gox) adjacent to the access edge; a first diffusion region adjacent to the access edge; a second diffusion region adjacent to the fusible edge (see N+ implant adjacent the Normal/Thinner Gox shown in fig. 16); and a thin gate oxide (Thinner Gox) over the active channel area adjacent to the fusible edge, the thin gate oxide having a lower breakdown voltage than the thick gate oxide for forming a conductive link between the polysilicon gate and the active channel area.

Re claim 24, a prima facie case of anticipation has been established because the claimed and prior art products are identical or substantially identical in structure and/or composition. *In re Best,* 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product."). *See also In re Spada,* 911 F.2d 705, 708-09, 15 USPQ2d 1655, 1657-58 (Fed. Cir. 1990).

Re claim 26, Peng discloses the polysilicon gate defines the active channel area between the fusible edge and the access edge, and the thick gate oxide and the thin gate oxide are disposed between the channel region and the polysilicon gate, the thick gate oxide extending

from the access edge to a predetermined length of the active channel area, and the thin gate oxide extending from the predetermined length of the active channel area to the fusible edge.

The recitation of claim 27 calling for, "the thick gate oxide portion includes a combination of an intermediate gate oxide and the thin gate oxide portion" fails to further limit the anti-fuse structure.

Re claim 28, Peng discloses the polysilicon gate (par. 86) has a first portion disposed over the thick gate oxide (Normal Gox) and located adjacent to the diffusion region for defining the active channel area, the access edge being defined by a first portion edge, and a second portion disposed over the thin gate oxide (Thinner Gox) and coupled to the first portion, the fusible edge being defined by a second portion edge, the second diffusion region being disposed between the fusible edge and the active channel area.

21. Claim 29 is rejected under 35 U.S.C. 102(e) as being anticipated by Peng.

Peng discloses in figs. 16 and 22-25 an anti-fuse transistor formed on a semiconductor material comprising: an active channel area (unnumbered); a polysilicon gate (par. 86) formed over the active channel area to define a fusible area (adjacent Thinner Gox), an access edge (adjacent Normal Gox) and an isolation edge (region between ldd spacer and Normal Gox); a thick gate oxide (Normal Gox) adjacent to the access edge; a diffusion region (N+ implant) adjacent to the access edge; a field oxide (ldd spacer) adjacent to the isolation edge; and a thin gate oxide (Thinner Gox) having a fusible area between the thick gate oxide and the isolation edge, the fusible area having a lower breakdown voltage than the thick gate oxide for forming a conductive link between the polysilicon gate and the active channel area.

Allowable Subject Matter

Claims 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANS
November 2, 2007

A. Sefer
Patent Examiner
Art Unit 2826